In the Claims:

1. (Currently Amended) Integrated circuit comprising a plurality of modules (M) for processing applications, each having a local memory (LM), said integrated circuit further comprising:

- a global memory (GM), which can be shared by said plurality of modules (M) ;

- [~~an~~] interconnected data communication paths ~~means~~ (IM) for interconnecting said modules (M) and said global memory (GM); and

- one memory managing unit (MMU) being associated to each of said modules (M), for determining whether said local memory (LM) provides sufficient memory space for the currently processed application and for, in response to the determining that there is not sufficient memory space, requesting a global buffer (FB) in said global memory (GM) to be exclusively reserved for the processing data of the associated module (M) and for, in response to the determining that there is not sufficient memory space, requesting a dedicated communication path between the associated module and the global buffer. ~~, if there is insufficient memory space available in the local memory (LM)~~.

2. (Currently Amended) Integrated circuit according to claim 1, ~~wherein~~

~~- said memory managing unit (MMU) requests a communication path between its associated module (M) and said global memory (GM),~~ wherein said communication path ~~having~~ has communication properties according to the required access to the global memory (GM).

3. (Original) Integrated circuit according to claim 1, further comprising

- a resource managing unit (RMU) for allocating memory space in said global memory (GM) according to the request of said memory managing unit (MMU).

4. (Original) Integrated circuit according to claim 3, wherein

- said resource managing unit (RMU) is adapted for setting [[~~a~~]] the communication path based on communication properties as requested by said memory managing unit (MMU).

5. (Original) Integrated circuit according to claim 4, further comprising

- an address translation unit (ATU) associated to each of said modules (M) for performing an address translation for data of an application, which are stored in said global buffer (FB) in said global memory (GM) .

6. (Previously presented) Integrated circuit according to claim 3, wherein

- said resource managing unit (RMU) is adapted to perform an access arbitration for said global memory (GM).

7. (Original) Integrated circuit according to claim 1, wherein

- said local memory (LM) comprises a prefetch buffer (PB) for prefetching data from said global buffer (FB).

8. (Currently Amended) Method for memory allocation in an integrated circuit comprising

a plurality of modules (M) for processing applications, wherein each module comprises a local memory (LM), ~~wherein said integrated circuit further comprises~~

a global memory (GM) being adapted to be shared between said plurality of modules (M), comprising the steps of:

- memory managing by determining whether said local memory (LM) provides sufficient memory space for the currently processed application and for, in response to the determining that there is not sufficient memory space, requesting a global buffer (FB) in said global memory (GM) to be exclusively reserved for the processing of one of said modules (M) and for, in response to the determining that there is not sufficient memory space, requesting a dedicated communication path between the associated module and the global buffer., ~~when there is not sufficient memory space available in said local memory (LM)~~.

9. (New) The integrated circuit of claim 3, wherein the RMU allocates memory space in said global memory in response to determining that there is adequate space in the global

memory to support the request and in response to determining that there is adequate transmission bandwidth to support the request.

10. (New) The integrated circuit of claim 1, wherein the MMU determines whether the LM provides sufficient memory space for the currently processed application by comparing the memory space in the LM to a predetermined value.

11. (New) The integrated circuit of claim 3, wherein the RMU provides an address of the global buffer to the MMU and wherein the MMU uses the provided address to perform address translation between an address provided by the associated module to the address of the global buffer.